Pokhara University

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| Level: Bachelor | Semester: Fall | Year : 2014 |
| Programme: BE | | Full Marks: 100 |
| Course: Computer Organization and Architecture | | Pass Marks: 45 |
| Time : 3hrs. |

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| *Candidates are required to give their answers in their own words as far as practicable.* |
| *The figures in the margin indicate full marks.* |
| Attempt all the questions. |

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|  | 1. Explain the assembling and compiling process with suitable examples. 2. What is system bus? Explain in details. | 7  8 |
|  | 1. A Computer system with an 8 bit address bus and an 8 bit data bus using isolated I/O. It has 16x8 ROM starting at the address 00H constructed using 8x8 chips; 64x8 of RAM starting at address 80 H constructed using 64x4 chips. There is an I/O device at 40 H. Show the design for the system. 2. How a 16×2 memory sub system can be constructed from two 8×2 ROM chip with low order interleaving and high order interleaving. Explain with diagram. | 8  7 |
|  | Design a CPU that meets the following specification:  It can access 64 bytes of memory each 8 bit wide. The CPU does this by outputting a 6 bit address on its output pin A{5…0}and reading 8 bit value from memory on its input D{7…0}. | 15 |
|  | 1. Describe the microinstruction format? Explain the horizontal and vertical micro code. 2. Write the RTL code for Booth’s algorithm. Using same code trace the multiplication of (-5) and (3). | 7  8 |
|  | 1. Show the layout of the cache for a CPU that can address 1M x 16 of memory; the cache holds 8k x 16 of data and has the following mapping strategies. Given the number of bits per location and total number of locations as well. 2. Fully Associative 3. Direct Mapped 4. Two – way associative 5. Describe the working principle of DMA with suitable diagram. | 8  7 |
|  | 1. What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Describe the solutions to correct data conflicts. 2. Describe different types of topologies of multiprocessor system. | 8  7 |
|  | Write short notes on: (**Any two**)   1. BCD Numeric Addition 2. DMA 3. VHDL | 2×5 |